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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/637,165	08/08/2003	Marc Tremblay	SUN-P9324	2937

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EXAMINER	
ZHE, MENG YAO	

ART UNIT	PAPER NUMBER
2195	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)
	10/637,165	TREMBLAY ET AL.
	Examiner	Art Unit
	MENGYAO ZHE	2195

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 February 2011*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-11 and 13-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-2, 4-11, 13-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)	
1) ☐ Notice of References Cited (PTO-892)	4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)	5) ☐ Notice of Informal Patent Application
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.	6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-2, 4-11, 13-20 are presented for examination.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 10, 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Herlihy et al., Patent No. 5,428,761 (hereafter Herlihy) in view of Ben-Meir et al., Patent No. 5,826,073 (hereafter Ben).

3. Herlihy, Ben-Meir were cited in the previous office action.

4. As per claims 1, 10, and 19, Herlihy teaches the invention as claimed including a method for executing a commit instruction to facilitate transactional execution on a processor, comprising:

Executing a block of instructions transactionally, wherein executing the block of instructions transactionally involves placing load-marks on cache lines from which data is loaded (Column 6, lines 34-35; Column 7, lines 1-14), placing store-marks on cache lines to which data is stored (Column 5, lines 45-49; Column 7, lines 1-14),

and placing transactional stores in a store buffer in the processor during the transaction (Column 6, lines 30-35; Fig 1, unit C), wherein the transactional stores are gated and not committed to memory from the store buffer during the transaction (Column 8, lines 4-8; Column 11, lines 27-30), wherein each entry in the store buffer include a data value for a store operation that is to be committed to a memory address (Column 5, lines 11-15).

Encountering the commit instruction during execution of a program, wherein the commit instruction marks the end of a block of instructions to be executed transactionally (Column 8, lines 16-28);

Upon encountering the commit instruction, successfully completing transactional execution of the block of instructions preceding the commit instruction, wherein successfully completing the transactional execution involves atomically committing changes made during the transactional execution by (Column 7, lines 25-58; Column 9, line 55):

Treating store-marked cache lines as locked, thereby causing other processes to wait to access the store-marked cache lines (Column 6, lines 34-40; Column 8, lines 4-8; Column 10, line 68-Column 11, line 5; Column 11, lines 52-54);

Committing store buffer entries generated during transactional execution to memory, wherein committing each store buffer entry involves removing the store-mark from, and thereby unlocking, a corresponding store-marked cache line (Column 6, lines 53-68);

Clearing load-marks from cache lines (Column 8, lines 24-25);

Committing register file changes made during transactional execution (Column 8, lines 1-8);

wherein changes made during the transactional execution are not committed to the architectural state of the processor until the transactional execution successfully completes. *(Column 8, lines 1-8).*

Herlihy does not specifically teach wherein the store buffer is a hardware structure separate from a register file and that register file changes are also committed during transactional execution.

However, Ben teaches that both a store buffer and a register file, and that each may separately committed to memory for the purpose of having different memories storing and processing different data (Fig 2; Column 11, line 60-Column 12, line 4: the store queue corresponds to the store buffer and the register file corresponds to applicant's register file).

It would have been obvious to one having ordinary skill in the art at the time of the applicant's invention to modify the teachings of Herlihy with the specifics of having both a store buffer and a register file, and that each may separately committed to memory, as taught by Ben, because it allows different memories to store and process different data for specialized purposes.

5. Claims 2, 4-7, 9, 11, 13-16, 18, 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Herlihy et al., Patent No. 5,428,761 (hereafter Herlihy) in view of Ben-Meir et al., Patent No. 5,826,073 (hereafter Ben) further in view of Rajwar et al. Patent No. 7,120,762, 10/10/2006, (hereafter Rajwar).

6. Rajwar was cited in the previous office action.

7. As per claims 2, 11, 20, Herlihy does not specifically teach wherein successfully completing the transactional execution involves atomically committing changes made during the transactional execution; and resuming normal non-transactional execution..

However, Rajwar teaches wherein successfully completing the transactional execution involves atomically committing changes made during the transactional execution; and resuming normal non-transactional execution for the purpose of continuing execution. *(Column 3, lines 15-17; Column 5, lines 57-60; Column 9, lines 45-50)*

It would have been obvious to one having ordinary skill in the art a the time of the applicant's invention to modify the teachings of Herlihy with wherein successfully completing the transactional execution involves atomically committing changes made during the transactional execution; and resuming normal non-transactional execution, as taught by Rajwar, because it allows for the program to continue executing.

8. As per claims 4, 13, Rajwar teaches

wherein if an interfering data access from another process is encountered during the transactional execution and prior to encountering the commit instruction, the method further comprises: discarding changes made during the transactional execution; and attempting to re-execute the block of instructions. *(Column 8, lines 50-65)*

9. As per claims 5, 14, Rajwar teaches

wherein for a variation of the commit instruction, successfully completing the transactional execution involves: atomically committing changes made during the transactional execution; and commencing transactional execution of the block of instructions following the commit instruction. *(Abstract and Column 9, lines 45-50, Column 3, line 15-17)*

10. As per claims 6, 15, Rajwar teaches

wherein potentially interfering data accesses from other processes are allowed to proceed during the transactional execution of the block of instructions. *(Column 2, lines 47-50)*

11. As per claims 7, 16, Rajwar teaches wherein the block of instructions to be executed transactionally comprises a critical section *(Column 2, lines 47-50)*

12. As per claims 9, 18, Rajwar teaches wherein the commit instruction is defined in a platform-independent programming language *(Column 10, lines 8-15)*

13. Claims 8 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Herlihy et al., Patent No. 5,428,761 (hereafter Herlihy) in view of Ben-Meir et al., Patent No. 5,826,073 (hereafter Ben) further in view of Rajwar et al. Patent No. 7,120,762, 10/10/2006, (hereafter Rajwar) further in view of Hecht et al, Pub. No. US 2003/0064808 (hereafter Hecht).

14. Hecht was cited in the last office action.

15. As per claims 8, 17, Rajwar teaches that the invention as he disclosed may be used on different computer architecture, meaning that they can be platform independent *(Column 10, lines 8-15)*

Rajwar does not teach the commit instruction being platform dependent. However, Hecht teaches a

> converter program that converts platform independent programs into platform dependent programs for the purpose of running the program on a specific type of machine *(Paragraph 14)*

It would have been obvious to one having ordinary skill in the art at the time of the invention to have modified the invention of Rajwar with

Converting the platform independent instruction to platform dependent instruction,

as taught by Hecht, because it allows the program to run on a specific type of machine.

Response to Arguments

16. Applicant's arguments filed on 2/14/2011 have been fully considered but are not persuasive.

17. In the remark, the applicant argued that:

i) Herlihy does not teach EACH and every entry in the store buffer includes a data value for a store operation that is to be committed to a memory address.

18. The Examiner respectfully disagrees with the applicant. As to point:

i) Herlihy teaches that a store buffer that loads data values into its entries so that the data values may be committed to memory address later. In the specific instance where processing requires enough data values such that all of the entries in Herlihy's data buffer becomes loaded, then all of the entries, i.e. EACH and every entry, in the data buffer will be committed to memory address.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MENGYAO ZHE whose telephone number is (571)272-6946. The examiner can normally be reached on Monday Through Friday, 7:30 - 5:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Mengyao Zhe/

/Meng-Ai An/
Supervisory Patent Examiner, Art Unit 2195